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EXAMINER
JONES, ERIC W

ART UNIT	PAPER NUMBER
2892	

NOTIFICATION DATE	DELIVERY MODE
11/24/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/584,052	POCAS ET AL.	
	Examiner	Art Unit	
	ERIC W. JONES	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-64* is/are pending in the application.

4a) Of the above claim(s) *1-26,46-52 and 58-64* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *27-45 and 53-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/14/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claim 27, 28, 30, 34-36 and 41are rejected under 35 U.S.C. 103(a) as being unpatentable over Neilson et al (6,054,369).

Re claim 27, Neilson et al disclose in FIGS. (2a or 2b or 2c or 2d) and 3 a method of sealing a first wafer (N^- Si 22 in FIGS. 2a-d) and a second wafer (N^+ Si below buffer layer 24 in FIGS. 2a-d) each made of semiconducting (silicon) materials, comprising:

implanting a metallic (Pt, Cu, Ni or Co centers "x" in FIGS. 2a-d) species in at least the first wafer (either first or second wafer or both), assembling the first wafer and

the second wafer by molecular bonding. (column 3, lines 47-67; column 4, lines 1-55; column 5, lines 5-22)

Neilson et al fail to explicitly disclose after the molecular bonding, forming a metallic ohmic contact including alloys formed between the implanted metallic species and the semiconducting materials of the first wafer and the second water, said metallic ohmic contact being formed at an assembly interface between the first wafer and the second wafer, wherein the forming includes causing the implanted metallic species to diffuse towards the interface between the first wafer with the second wafer and beyond the interface.

However, these limitations are obviously satisfied since Neilson et al disclose using suitable heat treatment can be performed after a molecular bond between the first and second wafers, which causes the metallic implant species to diffuse, both upward and downward, across the first and second wafer interface (20 in FIGS. 2a-d). Thus, the metallic species react with the silicon wafers to form metallic-silicon alloys which could functions as ohmic (metal-semiconductor: See Sze et al, 1st, 2nd or 3rd Ed. 1969, 1981, 2007; Chapter 3, Section 3.6) contacts. (column 3, lines 7-20; column 4, lines 25-55 column 5, lines 5-22)

Re claim 28, Neilson et al make obvious the claimed limitations of wherein the forming includes applying a heat treatment at a temperature equal at least to a formation temperature of the said alloys since it is disclosed that a suitable heat treatment can be performed after a molecular bond between the first and second wafers, which causes the metallic implant species to diffuse, both upward and

downward, across the first and second wafer interface (20 in FIGS. 2a-d), thus causing the metallic species react with the silicon wafers to form metallic-silicon alloys. (column 3, lines 7-20; column 4, lines 25-55 column 5, lines 5-22)

Re claim 30, Neilson et al disclose wherein the implanting includes implanting the metallic (Pt; column 4, lines 25-55) species at a dose of between 10^{14} and 10^{18} species/cm^2 (column 3, lines 47-65: a concentration of 10^{14} and 10^{19}/cm^3 corresponds to a dose of less than 10^{16} species/cm^2 as is evidenced by Bredthauer, column 3, lines 15-44)

Re claim 34, Neilson et al disclose the first wafer (N^- Si 22 in FIGS. 2a-d) and the second wafer (N^+ Si below buffer layer 24 in FIGS. 2a-d) being made from silicon. (column 5, lines 14-22)

Re claim 35, Neilson et al disclose the implanted species includes one of platinum, nickel, cobalt or copper. (column 4, lines 36-55)

Re claim 36, Neilson et al disclose at least one of the wafers is heterostructure (N^- Si 22 in FIGS. 2a-d comprises a dielectric on its top surface).

Re claim 41, Neilson et al disclose at least one of the wafers includes at least one circuit or circuit layer. (N^- Si 22 in FIGS. 2a-d comprises a dielectric and a polysilicon circuit layer on its top surface)

4. Claim 29, 42, 43, 45; 53 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Neilson et al in view of Bredthauer (4,742,017).

Re claim 29, Neilson et al disclose implanting the metallic species (Pt, Ni, Co or Cu) under a surface of the first wafer (N^- Si 22 in FIGS. 2a-d). (column 3, lines 47-67; column 4, lines 1-55)

Neilsonet al fail to disclose at a depth (Rp) of between 5 nm and 20 nm under a surface of the first wafer.

Bredthauer discloses in FIGS. 1-5 implanting a metallic (Pt) species a depth (Rp) of between 5 nm (50 Å) and 20 nm (200 Å) under a surface of a wafer (Si 21 in FIG. 1). (column 3, lines 15-44)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the metallic implant depth profile of Bredthauer with the method of Neilson et al to form Schottky barrier devices. (Bredthauer, Title and Abstract)

Re claim 42, 43 and 45, Neilson et al disclose forming of an insulating layer (N^- Si 22 in FIGS. 2a-d comprises a dielectric on its top surface) on the first wafer.

Neilson et al fail to disclose implanting includes using a mask to obtain local implantation zones; and before the implanting; and wherein the first wafer includes at least one insulating zone at a surface so as to obtain local implantation zones

Bredthauer discloses in FIGS 2, 3 and 5 forming of a patterned (mask) insulating layer (SiO_2 12 in FIG. 2) on a wafer (Si 21 in FIG. 1) before the implantation (Pt in FIG. 3) so as to obtain local implantation zones at and below a surface. (column 3, lines 15-44)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the patterned insulating of Bredthauer with the method of Neilson et al to perform selective implantation for a semiconductor device.

Re claim 53, Neilson et al disclose in FIGS. (2a or 2b or 2c or 2d) and 3 a method of sealing a first wafer (N^- Si 22 in FIGS. 2a-d) and a second wafer (N^+ Si below buffer layer 24 in FIGS. 2a-d) each made of semiconducting (silicon) materials, comprising:

implanting a metallic (Pt, Cu, Ni or Co centers "x" in FIGS. 2a-d) in at least the first wafer, at a depth under a surface of said first wafer, at a dose of between 1014 and 1018 species/cm2 (column 3, lines 47-65: a concentration of 10^{14} and $10^{19}/cm^3$ corresponds to a dose of less than 10^{16} species/cm^2 as is evidenced by Bredthauer, column 3, lines 15-44), assembling the first wafer and the second wafer by molecular bonding. (column 3, lines 47-67; column 4, lines 1-55; column 5, lines 5-22)

Neilson et al fail to explicitly disclose after the molecular bonding, forming a metallic ohmic contact including alloys formed between the implanted metallic species and the semiconducting materials of the first wafer and the second water, said metallic ohmic contact being disposed at an assembly interface between the first wafer and the second wafer, wherein the forming includes causing the implanted metallic species to diffuse towards the interface between the first wafer with the second wafer and beyond the interface.

However, these limitations are obviously satisfied since Neilson et al disclose using suitable heat treatment can be performed after a molecular bond between the first

and second wafers, which causes the metallic implant species to diffuse, both upward and downward, across the first and second wafer interface (20 in FIGS. 2a-d). Thus, the metallic species react with the silicon wafers to form metallic-silicon alloys which could functions as ohmic (metal-semiconductor: See Sze et al, 1st, 2nd or 3rd Ed. 1969, 1981, 2007; Chapter 3, Section 3.6) contacts. (column 3, lines 7-20; column 4, lines 25-55 column 5, lines 5-22)

With respect "at a depth of between 5 nm and 20 nm", Bredthauer discloses in FIGS. 1-5 implanting a metallic (Pt) species a depth (Rp) of between 5 nm (50 Å) and 20 nm (200 Å) under a surface of a wafer (Si 21 in FIG. 1). (column 3, lines 15-44)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the metallic implant depth profile of Bredthauer with the method of Neilson et al to form Schottky barrier devices. (Bredthauer, Title and Abstract)

Re claim 54, Neilson et al make obvious the claimed limitations of wherein the forming includes applying a heat treatment at a temperature equal at least to a formation temperature of the said metallic compounds since it is disclosed that a suitable heat treatment can be performed after a molecular bond between the first and second wafers, which causes the metallic implant species to diffuse, both upward and downward, across the first and second wafer interface (20 in FIGS. 2a-d), thus causing the metallic species react with the silicon wafers to form metallic-silicon alloys. (column 3, lines 7-20; column 4, lines 25-55 column 5, lines 5-22)

6. Claims 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Neilson et al in view of Kish, Jr. et al (5,783,477-prior art of record) and Abe et al (US 2002/0157790 A1-prior art of record).

Re claims 31-33, Neilson et al fail to disclose processing the first wafer to make all or part of a surface layer of the first wafer amorphous; and wherein the processing the includes depositing an amorphous material layer before and/or after implantation of the metallic species; wherein the processing includes implanting hydrogen.

Kish, Jr. et al disclose in FIG. 9 an amorphisation step before assembly to make all or part of the surface layer (93 or 95; column 8, lines 18-37) of the first wafer (semiconductor layer under 93 or 95) amorphous; and the amorphisation step comprising deposition of an amorphous material layer (91; column 8, lines 18-37); and the amorphisation step comprising a surface implantation (column 8, lines 18-37).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the amorphisation step before assembly to make all or part of the surface layer of the first wafer amorphous; and the amorphisation step comprising deposition of an amorphous material layer; and the amorphisation step comprising a surface implantation of Kish, Jr. et al with the method of Neilson et al to form an ohmic interface between unipolar semiconductor wafers. (Kish, Jr. et al Abstract)

Neilson et al and Kish, Jr. et al fail to disclose the amorphisation step comprising a surface implantation of hydrogen.

Abe et al disclose in FIGS. 2-3 the amorphisation step comprising a surface implantation, for example by hydrogen. (¶ [0064])

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the amorphisation step comprising a surface implantation, for example by hydrogen of Abe et al with the method of Neilson et al and Kish, Jr. et al to produce bonded wafers comprising an ion implantation of hydrogen without causing breakage of the wafers. (Abe et al Abstract)

7. Claims 37, 38 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Neilson et al in view of Kub et al (US 6,274,892 B1-prior art of record).

Re claims 37 and 44, Neilson et al fail to disclose thinning at least one of the wafers after the assembling or after the forming of the metallic compounds; and thinning the first wafer after implantation of the metallic species.

Kub et al disclose at least one of the wafers (80 in FIG. 2) being thinned, before the implantation and formation step of metallic compounds (Pt). (column 5, lines 62-67, column 6, lines 66-67 and column 7, lines 1-5)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the wafer thinning of Kub et al with the method of Neilson et al to form devices by low temperature direct bonding. (Kub et al, Title)

Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made to thin at least one of the wafers after the assembling or after the forming of the metallic compounds; and to thin the first wafer after implantation of the metallic species since the selection of any order of performing process steps is *prima facie* obvious in the absence of new or unexpected results. *In re Burhans*, 154

F.2d 690, 69 USPQ 330 (CCPA 1946); *In re Gibson*, 39 F.2d 975, 5 USPQ 230 (CCPA 1930). See MPEP § 2144.04.

Re claims 38, Neilson et al fail to disclose at least one of the wafers being is a debondable structure.

Kub et al disclose at least one of the wafers being a debondable structure. (wafers 80 and 95 are both debondable since the are bonded by low energy molecular (hydrophobic) bonding as is disclosed by the applicant; column 9, lines 37-61)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the debondable wafer(s) structure bonding of Kub et al with the method of Neilson et al to form devices by low temperature direct bonding. (Kub et al, Title)

8. Claims 39 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Neilson et al in view of Yu et al (US 6,410,371 B1-prior art of record).

Re claims 39 and 40, Neilson et al fail to disclose at least one of the wafers includes a weakening plane; and thinning the wafer including the weakening plane by fracture along the said weakening plane, after the assembling or after the forming of the metallic compounds.

Yu et al disclose in FIGS. 2 and 3A-3F at least one of the wafers (64 in FIG. 3E) including a weakening plane (weak zone); and the wafer including a weakening plane being thinned by fracture (broken) along the said weakening plane. (column 4, lines 19-43)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute the at least one of the wafers comprising a weakening plane of Yu et al for one of the wafers of Neilson et al; and to use the wafer comprising a weakening plane being thinned by fracture along the said weakening plane of Yu et al with the method of Neilson et al to form a semiconductor-on-insulator (SOI) wafer. (Yu et al Abstract)

9. Claims 55-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Neilson et al and Bredthauer as applied to claim 53 above, and further in view of Kish, Jr. et al (prior art of record) and Abe et al (prior art of record).

Re claims 55-57, Neilson et al fail to disclose processing the first wafer to make all or part of a surface layer of the first wafer amorphous; and wherein the processing the includes depositing an amorphous material layer before and/or after implantation of the metallic species; wherein the processing includes implanting hydrogen.

Kish, Jr. et al disclose in FIG. 9 an amorphisation step before assembly to make all or part of the surface layer (93 or 95; column 8, lines 18-37) of the first wafer (semiconductor layer under 93 or 95) amorphous; and the amorphisation step comprising deposition of an amorphous material layer (91; column 8, lines 18-37); and the amorphisation step comprising a surface implantation (column 8, lines 18-37).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the amorphisation step before assembly to make all or part of the surface layer of the first wafer amorphous; and the amorphisation step comprising deposition of an amorphous material layer; and the amorphisation step comprising a

surface implantation of Kish, Jr. et al with the method of Neilson et al to form an ohmic interface between unipolar semiconductor wafers. (Kish, Jr. et al Abstract)

Neilson et al and Kish, Jr. et al fail to disclose the amorphisation step comprising a surface implantation of hydrogen.

Abe et al disclose in FIGS. 2-3 the amorphisation step comprising a surface implantation, for example by hydrogen. (¶ [0064])

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the amorphisation step comprising a surface implantation, for example by hydrogen of Abe et al with the method of Neilson et al and Kish, Jr. et al to produce bonded wafers comprising an ion implantation of hydrogen without causing breakage of the wafers. (Abe et al Abstract)

Response to Arguments

10. Applicant's arguments with respect to claims 27-45 and 53-57 have been considered but are moot in view of the new ground(s) of rejection attributed to Neilson et al (6,054,369), and Bredthauer (4,742,017) and Kish, Jr. et al (5,783,477-prior art of record) and Abe et al (US 2002/0157790 A1-prior art of record) and Kub et al (US 6,274,892 B1-prior art of record).

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERIC W. JONES whose telephone number is (571)270-3416. The examiner can normally be reached on Monday-Friday 5:30AM-3:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571)272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Thao X Le/
Supervisory Patent Examiner, Art Unit 2892

/ERIC W JONES/
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11/17/2009